ABSTRACT OF THE DISCLOSURE

A memory device responsive to standby mode commands for reducing internal operational power on a memory device is disclosed. The memory device includes a circuit for reducing power during a standby mode with the circuit including a reference with at least first and second reference signals. The circuit also includes a switching device for switching between the first and second reference signals in response to the standby mode command and further controls an internal operational power regulator to adjust between normal and low-power outputs for further reducing the power to portions of the memory device.